Novel Slow-Wave Meander Lines Using Multilayer MMIC Technologies

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Abstract—**Slow-wave lines in a meander configuration, fabricated with multilayer MMIC technologies are proposed and their performance is investigated experimentally. Multilayer construction of capacitive triplate lines allows reduction of the chip area of periodic slow-wave line circuits. With this design, less than one half of the area of conventional straight slow-wave lines is required. Additionally, it permits higher frequency operation up to 40 GHz with a negligible dispersion.**

I. Introduction

REDUCTION of MMIC chip area is an important issue from a cost and reliability point of view. Passive devices, especially those designed with distributed transmission lines, are most consuming of MMIC real estate. Slow-wave lines with a very large "slow-wave factor" $\lambda 0/\lambda g$, have been investigated as a method to reduce the needed line length for a given insertion phase [1]–[5]. MIS and schottky-type slow-wave lines using semiconductor surface layers are inherently lossy [1], [2]. However, the crosstie coplanar waveguide proposed by Hasegawa *et al.* [3] and crosstie overlay coplanar waveguide proposed by Itoh *et al.* [4], [5] slow-wave lines exhibit less transmission line loss. This slow-wave structure consists of periodically connected high-impedance Z_H (inductive) and low-impedance Z_L (capacitive) transmission lines. The storage of electric and magnetic energy in separate spaces makes contributes to the slowly propagate wave.

Increasing both Z_H and decreasing Z_L is required to significantly increase the slow-wave factor mainly depends on $\sqrt{Z_H/Z_L}$. By spreading the gap width of coplanar waveguide Z_H is increased. Likewise, by increasing the strip conductor width of low-impedance lines, Z_L can be decreased. Obviously, both an increased slow-wave factor and size reduction cannot be accomplished simultaneously. To reduce the chip area of slow-wave line designs, we propose a new meander-like configuration using multilayer MMIC technologies [6], [7].

II. Circuit Configuration

Shown in Fig. 1(a) and (b) are top view and cross sectional views of newly proposed slow-wave lines in a meander configuration. Triplate transmission lines are used as capacitive low-impedance lines in this slow-wave lines. The ability to construct two layers of triplate lines connected with high-impedance lines through via holes make it possible to construct this structure. This structure is very effective in reducing the circuit size of periodic slow-wave lines in construct to conventional slow-wave lines with identical lengths.

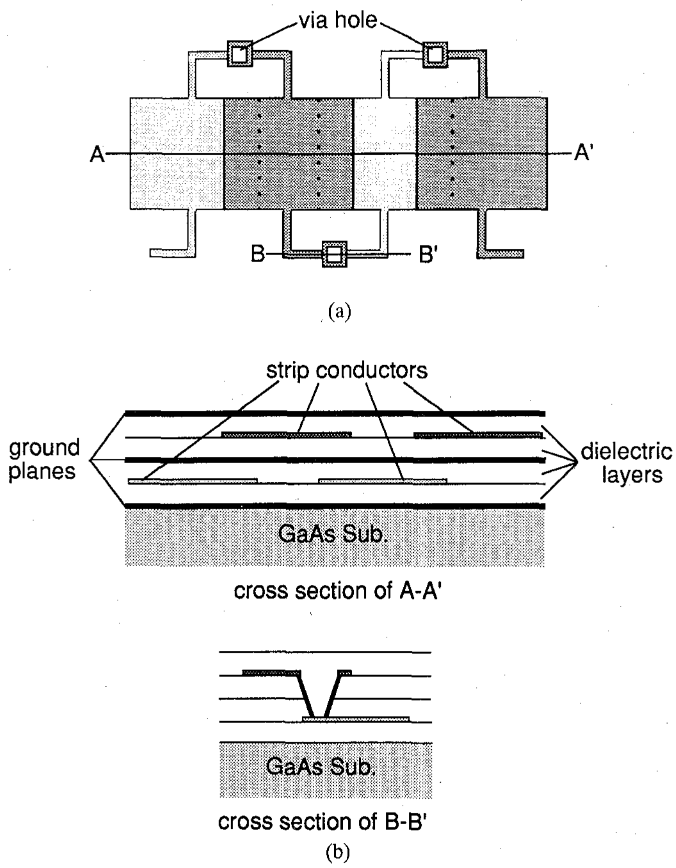

Fig. 1. Schematic views of meander slow-wave lines. (a) Top view with the ground planes removed. (b) Cross-sectional view.

By increasing the strip conductor width of triplate lines, the slow-wave factor is increased. By use of the triplate structure, it is possible to do this while at the same time decrease circuit size. This situation is facilitated by the center ground plane that effectively isolates the slightly overlapping lines. Thus, the circuit area has been effectively decreased while the slow-wave factor is simultaneously increased.

Higher frequency operation is also possible with this design. Moreover, this overlap feature reduces the lengths of inductive

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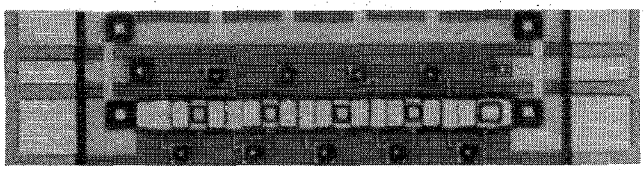


Fig. 2. Microphotograph of the meander slow-wave line.

high-impedance lines. This is beneficial to increasing the cut-off frequency of these periodic slow-wave lines, because the cut-off frequency is inversely proportional to the period length of the line [3], [4].

III. Design and Fabrication

Polyimide film is utilized as the dielectric layers and is deposited using multilayer MMIC technologies [6], [7]. The total dielectric film consists of four 2.5-μm thick layers, and fabricated on a GaAs substrate. The relative dielectric constant of the polyimide film is 3.3. All metalization thicknesses are 1 μm.

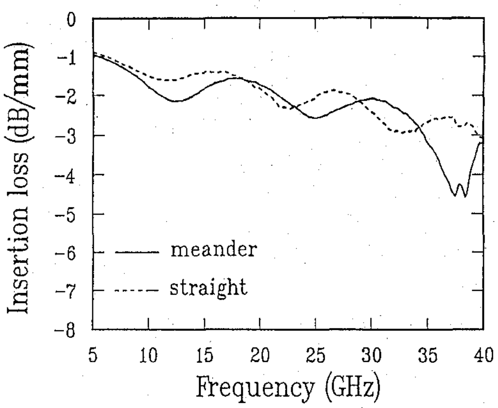
Fig. 2 shows a microphotograph of the meander slow-wave lines. Each section length of the low-impedance lines (L_L) is 60 μm and each section length of the high-impedance lines (L_H) is 90 μm not including the via hole area. In this study, the lines are designed with 10 periods, so the total line length shown in Fig. 2 is 1500 μm. However, the slow-wave lines are fabricated within a reduced area of 0.7 $\times$ 0.2 mm^2.

For comparison, a straight slow-wave line using only one layer triplate lines is also fabricated. This particular line has the crosstie coplanar waveguides replaced with triplate lines in the low-impedance sections [3], [4]. The lengths L_L, L_H, L_total of this structure are also 60 μm, 90 μm, and 1500 μm. The width between the ground planes of the coplanar waveguide is 200 μm. The total line length is 1.5 mm and the corresponding width is 0.2 mm.

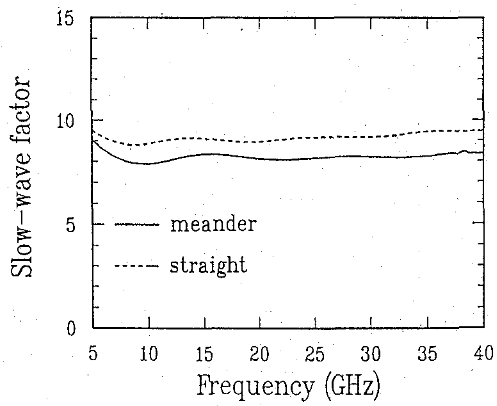
The strip conductor width of both meander and straight slow-wave lines is 100 μm for low-impedance lines and 5 μm for high-impedance lines. The predicted slow-wave factor of these slow-wave lines are at 20 GHz. These results are calculated by the methods proposed by Hasegawa and Itoh [3], [4].

IV. Experimental Results

Both slow-wave lines were measured by using on-wafer probes and an HP8510 A.N.A. Fig. 3 shows the both insertion loss and slow-wave factor as a function of frequency. The results are practically identical for both structures up to 40 GHz. Some difference between the results is due to the existence of via holes in the meander structure. Slightly decreasing the slow-wave factors of meander lines are thought to be the result of the decreased characteristic impedance of a high-impedance line with via hole pads in the meander structure caused by neighboring ground conductors. Offset in the insertion loss characteristic is thought to be caused by via pad discontinuities in the meander structure. The final chip area of the meander structure is less than one half that of the straight line's.



(a)



(b)

Fig. 3. Measurement results of both straight and meander slow-wave lines. (a) Insertion loss. (b) Slow-wave factor..

V. Conclusion

Slow-wave lines in a meander configuration, using the multilayer MMIC process, are newly designed and have been experimentally investigated. Multilayer construction of low-impedance triplate lines makes it possible to reduce the chip area and allow for high-frequency operation. The chip area of a meander structure is less than one half of that for a straight slow-wave line constructed with the same low- and high-impedance lines. This meander configuration is very useful for reducing the chip area of periodic slow-wave lines and shows potential for reducing the size of passive MMIC elements.

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